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Hierarchically Built Gold Nanoparticle Supercluster Arrays as Charge Storage Centers for Enhancing the Performance of Flash Memory Devices

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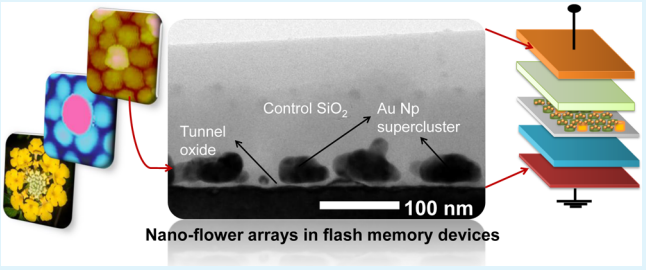
Supporting Information

ABSTRACT: Flash memory devices with high-performance levels exhibiting high charge storage capacity, good charge retention, and high write/erase speeds with lower operating voltages are widely in demand. In this direction, we demonstrate hierarchical self-assembly of gold nanoparticles based on block copolymer templates as a promising route to engineer nanoparticle assemblies with high nanoparticle densities for application in nanocrystal flash memories. The hierarchical self-assembly process allows systematic multiplication of nanoparticle densities with minimal increase in footprint, thereby increasing the charge storage density without an increase in operating voltage. The protocol involves creation of a parent template composed of gold nanoclusters that guides the self-assembly of diblock copolymer reverse micelles which in turn directs electrostatic assembly of gold nanoparticles resulting in a three-level hierarchical system. Capacitance−voltage ($C-V$) measurements of the hierarchical nanopatterns with a metal−insulator−semiconductor capacitor configuration reveal promising enhancement in memory window as compared to nonhierarchical nanoparticle controls. Capacitance−time ($C-t$) measurements show that over half the stored charges were retained when extrapolated to 10 years. The fabrication route can be readily extended to programmed density multiplication of features made of other potential charge storage materials such as platinum, palladium, or hybrid metal/metal oxides for next generation, solution-processable flash memory devices.



KEYWORDS: *block copolymer self-assembly, hierarchical structures, gold nanoparticles, flash memory, charge storage*

1. INTRODUCTION

Semiconductor devices for memory applications displaying high speed, longevity, and endurance are in great demand. Key factors that promote these attributes are small feature size, footprint, and retention of stored charges. The conventional continuous floating gate memory devices encounter limitations toward increasing charge density and their retention while also keeping with demands of ultrathin tunneling layer requirements.[1−3] When the thickness of the floating gate layer is scaled down, multiplication of nanoparticle density per unit area becomes difficult and thereby compromises on the number density of stored electrons, significantly affecting the device performance.[4] State-of-the-art memory devices based on silicon-oxide-nitride-oxide-silicon (SONOS) architectures suffer from limitations due to shallow trap levels that are vulnerable to easy leakage of stored charges, negatively impacting the memory retention.[5−7] In contrast, nanocrystal-based memories offer multibit storage capability and deep trap states that better address the leakage issue.[8,9] More importantly, they can be fabricated with greater process flexibility to cater to progressive needs of scaling device dimensions in accordance with specifications targeted by the International Technology Roadmap for Semiconductors (ITRS).[1] Consequently, metal nanocrystal based nonvolatile memories have become increasingly important relative to their conventional floating gate devices[10] or the charge trap flash SONOS devices[7,9] since they

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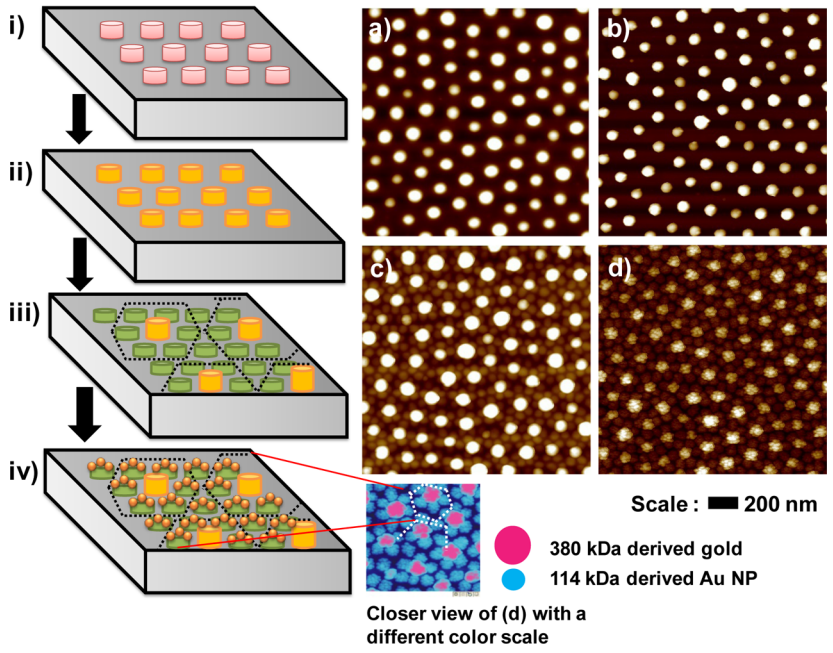

Figure 1. Process steps toward fabricating Au NP hierarchical supercluster using block copolymer templates is illustrated in schematics (i–iv) along with the corresponding AFM images (a–d). (i, a) Spin-coated PS-*b*-PVP (380 kDa) reverse micelles. (ii, b) In situ synthesis of parent gold template (*A*-only arrays). (iii, c) Second-level hierarchy obtained after spin coating 114 kDa reverse micelles of PS-*b*-PVP onto the parent gold templates (BC_{18} arrays). (iv, d) Electrostatic self-assembly of citrate-stabilized, preformed Au NPs giving rise to ternary hierarchy ($AC_{17}(BC_{18})_{5.5}$ supercluster arrays).

offer numerous advantages in terms of higher density of states, better size tunability, and scalability to optimize device characteristics.[11−13]

The performance of nanocrystal memory devices critically depends on the size, density, distribution, and spatial arrangement of the constituent nanoclusters.[2,8,14,15] Various techniques have been employed to fabricate metal nanocrystals as the charge storing layer on Si surfaces such as thin film deposition and annealing,[16−18] in situ synthesis within block copolymer templates,[12,19] binding of metal nanoparticles on surfaces using covalent assemblies,[20,21] and layer-by-layer assembly.[13,22] Directed metal nanoparticle deposition using block copolymer templates in a hierarchical fashion has received special attention due to the ability of templates to exert a definite and precise control over the geometric attributes such as the nanoparticle density, feature-to-feature interval, periodicity, and spacing of the resulting assemblies at every level.[23−25] The use of block copolymer templates offer solutions that overcome limitations of nonhomogenous size and spatial distributions, agglomeration, and poor batch-to-batch reproducibility commonly encountered in nanoparticle assemblies.

Here, we adopt a hierarchical self-assembly route that employs block copolymer templates in a multilevel assembly scheme that enables programmable increase in nanoparticle densities. The approach benefits from the toolbox of capabilities available at disposal of self-assembly to produce economically viable, high-resolution patterns of range of metals such as Pt, Ag, and Au[19,26−30] or semiconducting materials such as ZnO or TiO_2[31−34] with ease and scalability in fabrication.[23,24,35,36] The advantages of uniformity in geometries of nanopatterns and the hierarchical density multiplication is found to translate into enhanced device performance through greater charge storage at lower bias voltage and longer retention. Density multiplication is achieved by the formation of gold nanoparticle super clusters (cluster of clusters). The device characteristics are highly reproducible over the entire device area and the resulting supercluster arrays exhibit a 1.5-fold increase in charge storage density in comparison with the memory window obtained for the parent template.

2. EXPERIMENTAL SECTION

2.1. Materials. Acetone, 2-propanol, and *m*-xylene were obtained as anhydrous solvents with purity >99% from Sigma-Aldrich Pte Ltd. Hydrogen tetrachloroaurate(III) trihydrate ($HAuCl_4{\cdot}3H_2O$) (99.9%, Aldrich) and sodium citrate (Sigma) were used as received. The *p*-type silicon wafers with thermally grown oxide were obtained from Globalfoundries Singapore Pte Ltd., Singapore. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy (AFM) were purchased from Nanosensors (Neuchatel, Switzerland).

2.2. Methods. The silicon substrates were cleaned by ultrasonicating successively in acetone and 2-propanol for 15 min and finally treated with UV/ozone (SAMCO UV-1, SAMCO Inc., Kyoto, Japan) for 10 min. The thickness of the oxide layer was measured using ellipsometry (Wvase 32, J.A. Woollam Co., Inc., Lincoln, NE). The gold nanoparticle supercluster was fabricated in three steps as described elsewhere.[24] Briefly, reverse micelle of polystyrene-*block*-poly(2-vinylpyridine) (PS-*b*-PVP) (Mw = 190 000-*b*-190 000 g mol^{-1}, Polydispersity index = 1.1) were self-assembled on the Si surface by spin coating the polymer from *m*-xylene solutions of 0.5% (w/w) concentration, at 6000 rpm spin speed. The micelle arrays were incubated in 5 mg mL^{-1} $HAuCl_4$ aqueous solution for 15 min. The polymer template was then removed using O_2 plasma reactive ion etch (RIE) (Oxford plasmalab 100, Oxfordshire, UK) for 10 min duration (at 30 W, 65 mTorr, 20 sccm O_2). Schematic for the formation of the parent gold template which occupies the first level of hierarchy is shown in Figure 1 (illustrated in steps (i) and (ii)). After the RIE process, a second layer of PS-*b*-PVP (Mw = 57 000-*b*-57 000 g mol^{-1}, PDI = 1.1) from *m*-xylene of 0.5% (w/w) concentration was spin-coated at 3000 rpm, giving rise to the second level of hierarchy. Subsequently, the sample was immersed in an aqueous suspension of citrate-stabilized preformed Au NPs for 1 h duration to direct the

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electrostatic self-assembly of the negatively charged Au NPs on to the positive nitrogen-rich cores of the reverse micelles completing the third level of hierarchy. The stable colloidal Au NPs were prepared according to a standard procedure reported elsewhere.[37] Briefly, in a round-bottom flask fitted with a reflux condenser, 60 mL of 1 mM $HAuCl_4$ was boiled with vigorous stirring. Later, 12 mL of 38.8 mM sodium citrate was added to the vortex of the solution that eventually changed the color of the solution to red wine. The solution was then cooled before being used. The electrostatic adsorption of the citrate-stabilized Au NPs on to the micelles was followed by another oxygen plasma exposure to remove the polymer templates, thus completing the fabrication of superclusters of gold nanoparticles. The pattern characteristics, viz. the mean height, width, and center-to-center spacing of reverse micelle arrays at various levels of hierarchy were characterized using tapping mode AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and scanning electron microscopy (SEM) (FESEM 6700F, JEOL, Tokyo, Japan). The plan view and cross-sectional view of the gold nanoparticle supercluster were obtained using transmission electron microscopy (TEM) performed using a Philips CM300 TEM operating at 300 kV. X-ray photoelectron spectroscopy (XPS) (AXIS Ultra^{DLD}, Kratos Analytical Ltd., Manchester, UK) measurements were performed using monochromatized Al Kα X-ray source (1486.71 eV photons) at a constant dwell time of 100 ms and pass energy of 40 eV to confirm the absence of polymer after fabrication (Figure S1 of the Supporting Information). The SiO_2 control oxide was deposited using a SiO_2 target (99.995% pure) with a copper backing plate in an unbalanced magnetron sputtering system (Nanofilm Technologies International Pte. Ltd., Singapore). The variation in film uniformity was typically less than 5%. All depositions were carried out at a chamber base pressure of less than 10^{-6} Torr; 120 nm thick Au contact electrodes were then deposited through a metal stencil mask of 0.3 mm diameter and spacing of 1 mm. The electrode deposition was carried out by line of sight deposition of gold using an electron beam evaporator. A Pt back electrode was sputtered on the backside of the silicon substrate after removing the native oxide using sandpaper. The C–V measurements were performed using the HP4284A precision LCR meter (Hewlett-Packard, US) under a measurement frequency of 100 kHz. C–t measurements were performed using the same instrument by monitoring the capacitance as a function of time at the V_{FB}.

3. RESULTS AND DISCUSSIONS

3.1. Hierarchical Self-assembly of Au Nanoparticle Supercluster Arrays. The hierarchical assemblies of gold nanoparticle superstructures were fabricated by adapting a sequential self-assembly process that we recently reported.[24] The process makes use of the features at each level of hierarchy as template to direct self-assembly at the consequent level. The first level of hierarchy consists of two-dimensional quasi-hexagonally organized gold nanoparticle arrays "*A*" derived through in situ synthesis within PS-*b*-PVP reverse micelle arrays (380 kDa, f_{PS} ~0.5) coated on the surface.[24,29] These gold particles exhibit feature width of ~90 nm and a periodicity of ~220 nm, and serve as templates to guide capillary self-assembly of reverse micelles of PS-*b*-PVP (114 kDa, f_{PS} ~ 0.5), "*B*" to form *ABx*-type binary superstructures (Figure 1).

The capillary self-assembly is realized simply by spin coating the solution of reverse micelles from *m*-xylene on top of the gold nanoparticle arrays. We had shown earlier that the mean value of x in *ABx* features can be systematically controlled by varying feature separations in *A* arrays.[24] For the nanoparticle assemblies intended in the report, we employed *A* feature separations larger than twice the diameter of *B*, allowing realization of $AB_{5.5}$ arrays. The $AB_{5.5}$ arrays were subsequently used as templates to guide electrostatic attachment of preformed citrate-stabilized gold nanoparticles "*C*" to achieve the third level of hierarchy. The electrostatic self-assembly is enabled through the positively charged PVP core present in *B* features that attract negatively charged citrate-stabilized Au nanoparticles from the solution phase. The preformed citrate-stabilized Au NPs exhibited a diameter of ~11.7 nm as shown in the inset of Figure 2 (a).

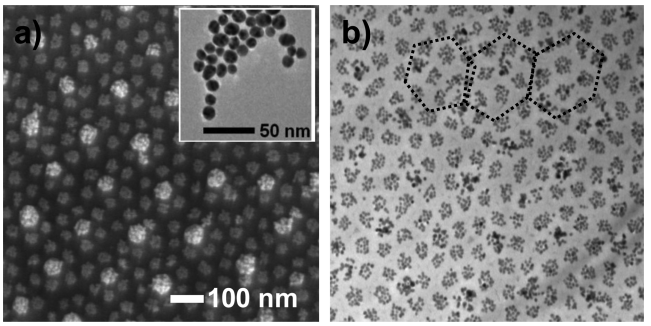

Figure 2. (a) FESEM image of the $AC_{17}(BC_{18})_{5.5}$ supercluster arrays and the corresponding (b) plan view TEM image. Inset in (a) shows the TEM image of the preformed citrate-stabilized Au nanoparticles.

Our earlier studies showed that the number of *C* features adsorbing to each *B* feature was determined by the latter's surface area, and could be estimated to be ~18 particles.[38] The *C* features were found to adsorb not only on *B* but also to *A* features. The SEM statistics showed about 17 nanoparticles of *C* were adsorbed per *A* feature. This was likely due to deposition of the block copolymers also on *A* features during the formation of binary hierarchies that imparted the *A* features with a partial positive charge. The resulting ternary assemblies therefore correspond to a configuration of $AC_{17}(BC_{18})_{5.5}$, with excellent uniformity over the entire coated area (1.5 cm × 1.5 cm) (Figure 2).

3.2. Supercluster-MIS (Metal–Insulator–Semiconductor) Device Characteristics. The charge storage and retention performance of the hierarchical nanoparticle assemblies was investigated by incorporating them within a metal–insulator–semiconductor (MIS) capacitor device with Pt/*p*-Si/SiO_2/$AC_{17}(BC_{18})_{5.5}$ superstructures/SiO_2 (50 nm)/Au stack structure (Figure 3).

Briefly, the $AC_{17}(BC_{18})_{5.5}$ superstructures were fabricated on *p*-Si substrates consisting of thermally grown tunneling oxide

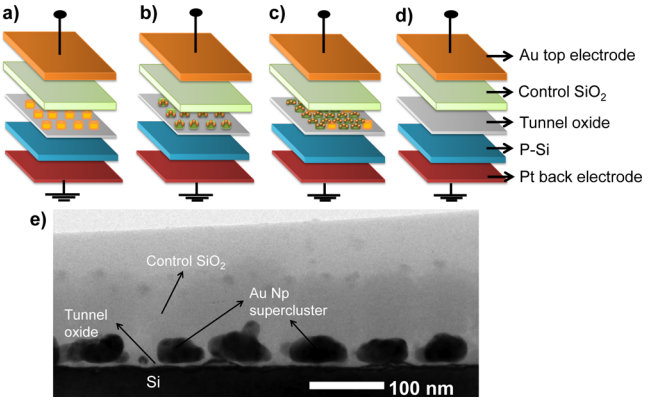

Figure 3. Schematic of the MIS capacitor test structure incorporating (a) *A*-only features, (b) BC_{18} arrays, (c) $AC_{17}(BC_{18})_{5.5}$ superclusters, and (d) control structure without charge storage centers. (e) Cross-section TEM image showing the supercluster test device structure.

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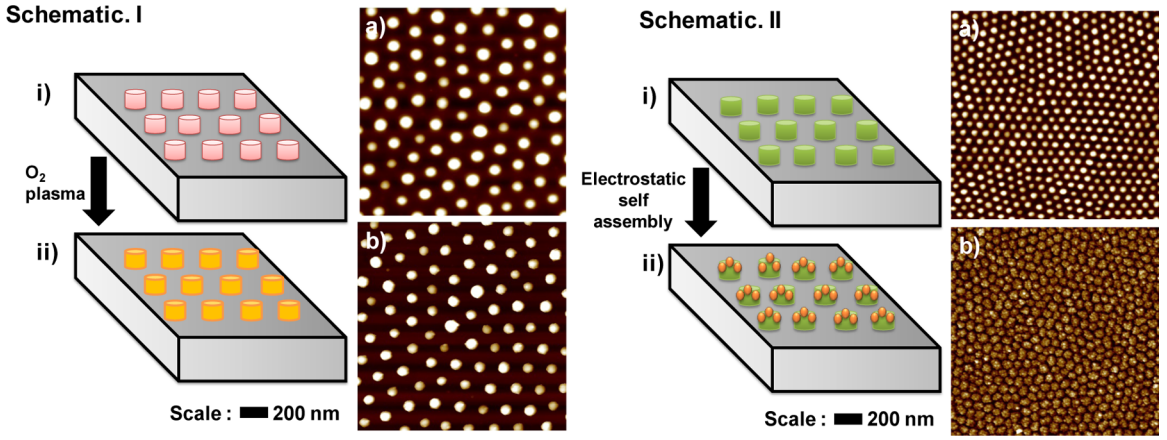

Figure 4. Left: Process steps toward fabricating parent gold template are illustrated in schematic I (i, ii) along with the corresponding AFM images (a, b). (i, a) The spin-coated PS-*b*-PVP (380 kDa) reverse micelles that acted as anchor points for (ii, b) in situ synthesis of *A*-only gold arrays. Right: Illustration of process steps toward fabricating 114 kDa derived Au NP cluster of type BC_{18} as control with the corresponding AFM images (a, b). (i, a) The spin-coated PS-*b*-PVP (114 kDa) reverse micelles which direct the (ii, b) electrostatic self-assembly of citrate-stabilized preformed Au NP to form cluster arrays.

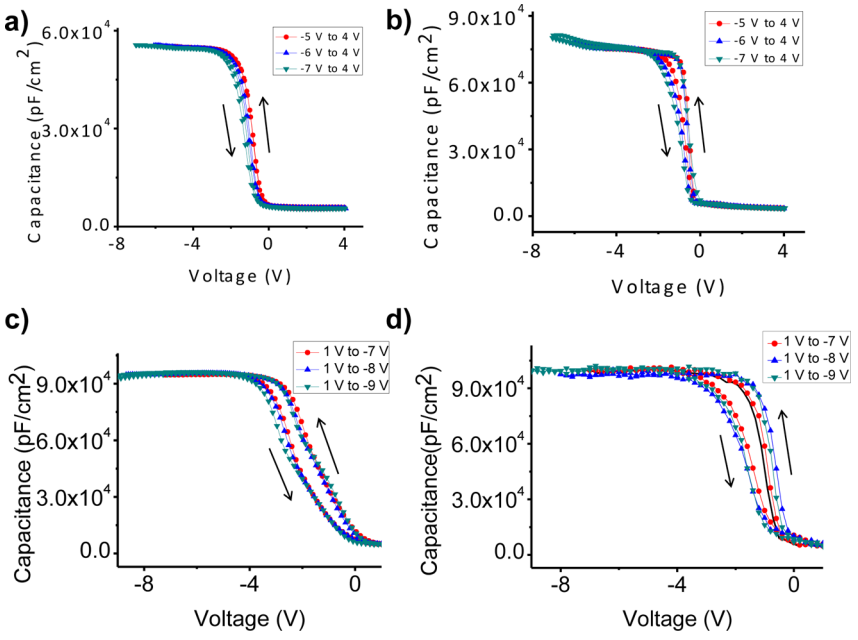

Figure 5. Capacitance–voltage characteristics of the (a) control device with no charge storage centers, (b) BC_{18} gold nanoparticle cluster, (c) *A*-only gold features, and (d) $AC_{17}(BC_{18})_{5.5}$ superclusters arrays with three levels of hierarchy.

with thickness of 3 nm and subsequently coated with a silicon dioxide of 50 nm thickness by radio frequency sputtering. Due to the isotropic nature of the sputter deposition, the SiO_2 film completely covered the nanoparticle assemblies (refer to TEM image in Figure 3), preventing any shorting with the top electrode. The substrate was annealed after deposition of the control oxide followed by deposition of Au and platinum electrodes (cf. Methods section for electrode fabrication details). To decipher the enhancement to charge storage capability by the superclusters, MIS capacitors incorporating the $AC_{17}(BC_{18})_{5.5}$ were compared against control MIS capacitors incorporating *A*-only and BC_{18}-only arrays as controls (Figure 4).

3.3. Capacitance–Voltage (*C*–*V*) Characteristics. *C*–*V* hysteresis curves of the MIS memory device containing no metal structures, or incorporating *A*-only, BC_{18}-only, and $AC_{17}(BC_{18})_{5.5}$ superstructure arrays are shown in Figure 5. The gate bias voltage was swept more toward negative potential. For any increase in the negative gate potential (until −7 V), the control sample (without nanoclusters) showed little or negligible flat band voltage (V_{FB}) shift. In all the other three cases, the observed counterclockwise hysteresis demonstrated net positive charging or hole injection into the charge storage centers (CSCs) due to net hole trapping from the substrate accumulation layer into the gold nanofeatures. The MIS test device with BC_{18} arrays showed a counter clockwise hysteresis with the memory window of 0.62 V when the applied negative operating potential was 7 V. Further increase in the voltage did not increase the memory window which is indicative of the saturation of the CSCs with charge carriers. The *A*-only and $AC_{17}(BC_{18})_{5.5}$ arrays showed memory windows or V_{FB} shifts of 0.82 and 1.13 V, respectively, when operated at 9 V. It could be inferred that increasing amounts of charges tunnel through the oxide layer and get stored in the

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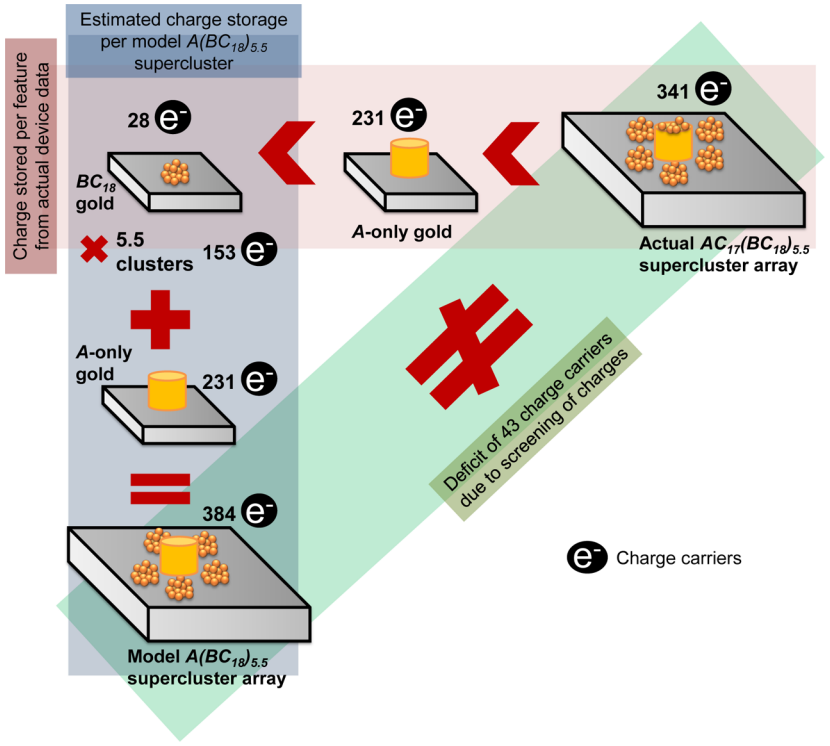

Figure 6. Illustration of the charge storage capacity of the actual $AC_{17}(BC_{18})_{5.5}$ supercluster device compared with the model $A(BC_{18})_{5.5}$ array.

CSCs when the applied negative bias is increased and the $C-V$ curve shifts more toward negative voltages. The memory window did not expand or shift when the applied voltage shifted more toward positive potential, suggesting that the charges trapped are indeed holes[39] (refer to Figure S2 of the Supporting Information for the $C-V$ plot for positive bias voltages).

The observed hysteresis behavior can be explained based on the charging/discharging of the nanoparticle charge storage centers. The density of the charge carriers can be estimated using the following equation:[40] $Q = (C_d{*}V_{FB})/(qa)$, where C_d is the capacitance of the dielectric stack layer, V_{FB} is the flat band voltage shift, q is the charge of an electron, and a is the area of the electrode. In the MIS device constructed using BC_{18} clusters, a flat band voltage shift of 0.62 V for a sweep voltage of 7 V is observed and the charge carrier density is estimated to be 3.14×10^{11} cm^{-2}. No further widening of the memory window was observed for sweep voltages of 8 or 9 V, indicating that the CSCs are saturated. For the V_{FB} shift of 0.82 at 9 V sweep, the MIS capacitor comprising the A-only arrays exhibited an estimated charge carrier density of 4.85×10^{11} cm^{-2}. On the basis of the assumption that the charges are distributed evenly, the charges stored in the control arrays can be calculated to be ~28 holes per BC_{18} cluster and ~231 holes per A feature.

An estimate of the charge storage capacity of $AC_{17}(BC_{18})_{5.5}$ supercluster features can be arrived at from $C-V$ measurements performed on A-only and BC_{18}-only arrays. From the supercluster device hysteresis, the number of charge carriers estimated increases to 5.06×10^8 when the shift in V_{FB} is 1.13 at 9 V sweep (Figure 5 d). Given the density of the features in the A-only array is the same as that in $AC_{17}(BC_{18})_{5.5}$ arrays, the number of charge carriers stored by A features of $AC_{17}(BC_{18})_{5.5}$ arrays is assumed to be the same as that in the control device which is ~231 holes per gold feature. This implies that about 3.43×10^8 charge carriers of the total 5.06×10^8 charge carriers are stored in the first level of hierarchy. The remaining 1.63×10^8 charge carriers are expected to be shared between the BC_{18} clusters and the ~17 features of C that sit on top of A features. The total number of C features in the entire supercluster is $\sim 1.72 \times 10^8$ which in turn accounts for the storage of ~1 charge carrier per feature. Thus, this accounts for the storage of ~341 holes per $AC_{17}(BC_{18})_{5.5}$ supercluster determined experimentally (refer to Supporting Information for the calculation of charge storage density).

To bring out the significance of this estimate, we compared the charge storage per supercluster to a model supercluster of type $A(BC_{18})_{5.5}$ (Figure 6).

Since the gold nanoparticle density is lesser (model excludes the C_{17} features on top of A), it is obvious to expect lesser holes to be stored per $A(BC_{18})_{5.5}$ supercluster. However, the estimation yielded a value of 384 holes stored per supercluster which is 43 holes greater than the experimentally observed charge carrier densities. The reason for the reduction in the experimentally determined charge carrier densities compared to the estimated values from the model can be understood as follows. Since the $AC_{17}(BC_{18})_{5.5}$ supercluster have gold nanofeatures with two different sizes (A, C), charges injected during programming can be expected to preferentially reside within the larger sized A particles, due to their proximity to the silicon surface, higher density of states, and lower Coulombic barrier.[41] However, due to the repulsive forces between adjacent C features (negatively charged citrate-Au nanoparticles) present in BC_{18} clusters, any further injection of charges into the supercluster is screened which could account for the deficit of 43 charge carriers and the deviation from the ideal case scenario. This reasoning is consistent with reports that have shown that the presence of an electrostatic barrier during charge injection would lower the amount of charge carriers stored in the CSCs.[15,41] However, despite the screening

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effect, the fabrication of the supercluster in our work has facilitated multiplication of the particle density and thereby the charge storage density. This is evident from the fact that a larger hysteresis is observed in the case of $AC_{17}(BC_{18})_{5.5}$ arrays as compared to *A*-only and BC_{18}-only arrays.

The V_{FB} shift of various device structures along with their charge storage densities is summarized in Table 1.

Table 1. Summary of the Performance of Devices Containing Charge Storage Centers of Type *A*-Only Arrays, BC_{18}-Only Arrays, and $AC_{17}(BC_{18})_{5.5}$ Supercluster Arrays

device type	control (no charge storage centers)	*A*-only array	BC_{18} array	$AC_{17}(BC_{18})_{5.5}$ supercluster array
V_{FB} (V)	0.16	0.82	0.62	1.13
Q(assembly) (cm^{-2})	NA	4.85×10^{11}	3.14×10^{11}	7.16×10^{11}
charge carriers stored per feature	NA	231	28	341

3.4. Capacitance–Time Characteristics. Capacitance decay measurement was performed to assess the charge retention capacity of the supercluster MIS capacitor device after charging it at V_G of −9 V for 30 s. A voltage equal to the flat band voltage (V_{FB} = −0.91 V) was applied to the top electrode for 10 000 s with the back electrode grounded. As could be observed from the *C*–*t* plot in Figure 7a, the supercluster device shows good retention characteristics retaining over 77% of the injected charges after 10 000 s.

The well-isolated flowerlike patterns inhibit any lateral charge conduction and thereby reduce any charge leakage from the gold clusters.[2,42] The *C*–*t* plot is further extrapolated to evaluate the retention trend after 10 years and it could be inferred that the supercluster device could still retain about half the injected charges. While the retention characteristics of the previously reported nanoparticle-based memory devices[42,43] are affected through lateral charge conduction, the characteristics are better in the supercluster-based MIS devices. Furthermore, they can be fabricated with a vastly simplified, economical, tunable, and scalable method.

4. CONCLUSIONS

This work presents a novel route to fabricate large-scale hierarchical flowerlike gold supercluster arrays with high particle and pattern densities for application in memory and other nanoelectronic devices. Use of electrostatic self-assembly of Au NPs in a layer-by-layer fashion driven by block copolymer-based hierarchical self-assembly for particle density multiplication in flash memory devices is reported. The significance of the hierarchical superclusters can be realized from the observation of increased charge storage and longer retention characteristics in the test devices made possible through particle density multiplication, a unique feature offered by the superclusters. The protocol is simple and involves a cost-effective polymer-based approach. The process is amenable to formation of a fourth level of hierarchy using metal nanocrystals or a combination of materials to form hybrid supercluster arrays to increase nanoparticle densities even further. Process variables such as the periodicity of the template features, edge-to-edge spacing, and levels of hierarchy can be optimized to design and obtain a variety of nanocluster arrays. The protocol also offers handles to enable scaling down of the devices in accordance with the ITRS as the approach is completely based on block copolymer self-organization which is widely considered to be the tool of the future for fabricating sub-10 nm electronic devices such as advanced transistors and diodes. Moreover, the process is generic in nature and can be easily adapted to form superclusters of metals and metal oxides which can be multicomponent in nature.

■ ASSOCIATED CONTENT

Supporting Information

XPS analysis of the patterns and the calculation of charge storage density. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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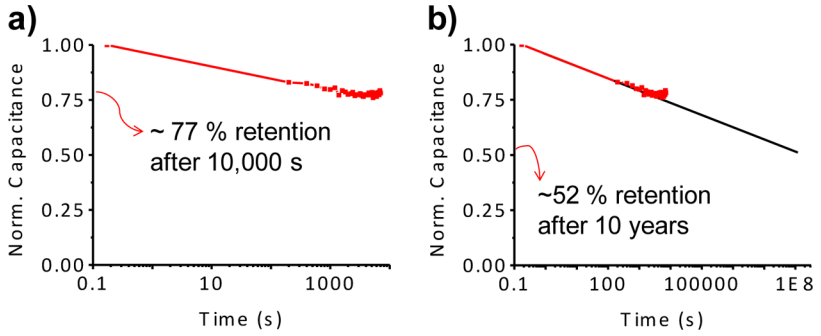

Figure 7. (a) Capacitance decay characteristics of the $AC_{17}(BC_{18})_{5.5}$ superclusters for 10 000 s and (b) extrapolated for 10 years.

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ACS Appl. Mater. Interfaces 2015, 7, 279–286

REFERENCES

(1) International Technology Roadmap for Semiconductors, Front End Processes (FEP), 2013 Tables. http://www.itrs.net/Links/2013ITRS/Home2013.htm. Accessed April 30, 2014.

(2) Min, S.; Tsu-Jae, K. Impact of Crystal Size and Tunnel Dielectric on Semiconductor Nanocrystal Memory Performance. *IEEE Trans. Electron Devices* **2003**, *50*, 1934−1940.

(3) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U. I.; Yoo, I.-K.; Kim, K. A Fast, High-Endurance and Scalable Non-volatile Memory Device Made From Asymmetric Ta_2O_{5-x}/TaO_{2-x} Bilayer Structures. *Nat. Mater.* **2011**, *10*, 625−630.

(4) Kuesters, K. H.; Ludwig, C.; Mikolajick, T.; Nagel, N.; Specht, M.; Pissors, V.; Schulze, N.; Stein, E.; Willer, J. Future Trends in Charge Trapping Memories. In *2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, Shanghai, China, Oct 23−26, 2006; Tang, T.-A., Ru, G.-P., Jiang, Y.-L., Eds.; IEEE: Piscataway, NJ, 2006; pp 740−743.

(5) Tsai, W. J.; Gu, S. H.; Zous, N. K.; Yeh, C. C.; Liu, C. C.; Chen, C. H.; Tahui, W.; Pan, S.; Chih-Yuan, L. Cause of Data Retention Loss in a Nitride-Based Localized Trapping Storage Flash Memory Cell. In *2002 IEEE International Reliability Physics Symposium Proceedings, 40th Annual*, Dallas, Texas, Apr 7−11, 2002; IEEE: Piscataway, NJ, 2002; pp 34−38.

(6) Ye, Z.-H.; Chang-Liao, K.-S.; Liu, T.-C.; Wang, T.-K.; Tzeng, P.-J.; Lin, C.-H.; Tsai, M.-J. A Novel SONOS-type Flash Device with Stacked Charge Trapping Layer. *Microelectron. Eng.* **2009**, *86*, 1863−1865.

(7) Joo Hyung, Y.; Hyun Woo, K.; Dong Hun, K.; Tae Whan, K.; Keun Woo, L. Effect of the Trap Density and Distribution of the Silicon Nitride Layer on the Retention Characteristics of Charge Trap Flash Memory Devices. *Int. Conf. Simul. Semicond. Processes Devices (SISPAD)* **2011**, 199−202.

(8) Liu, Z.; Lee, C.; Narayanan, V.; Pei, G.; Kan, E. C. Metal Nanocrystal Memories. I. Device Design and Fabrication. *IEEE Trans. Electron Devices* **2002**, *49*, 1606−1613.

(9) Lee, J.-S. Progress in Non-Volatile Memory Devices Based on Nanostructured Materials and Nanofabrication. *J. Mater. Chem.* **2011**, *21*, 14097−14112.

(10) Hanafi, H. I.; Tiwari, S.; Khan, I. Fast and Long Retention Time Nano-Crystal Memory. *IEEE Trans. Electron Devices* **1996**, *43*, 1553−1558.

(11) Aaron, V. Y.; Leburton, J. P. Flash Memory: Towards Single-Electronics. *Potentials, IEEE* **2002**, *21*, 35−41.

(12) Lee, J.-S. Recent Progress in Gold Nanoparticle-Based Non-Volatile Memory Devices. *Gold Bull.* **2010**, *43*, 189−199.

(13) Lee, J.-S.; Cho, J.; Lee, C.; Kim, I.; Park, J.; Kim, Y.-M.; Shin, H.; Lee, J.; Caruso, F. Layer-by-Layer Assembled Charge-Trap Memory Devices with Adjustable Electronic Properties. *Nat. Nano* **2007**, *2*, 790−795.

(14) Lee, C.; Meteer, J.; Narayanan, V.; Kan, E. C. Self-Assembly of Metal Nanocrystals on Ultrathin Oxide for Nonvolatile Memory Applications. *J. Electron. Mater.* **2005**, *34*, 1−11.

(15) Diao, P.; Guo, M.; Zhang, Q. How Does the Particle Density Affect the Electrochemical Behavior of Gold Nanoparticle Assembly? *J. Phys. Chem. C* **2008**, *112*, 7036−7046.

(16) Tsoukalas, D.; Dimitrakis, P.; Kolliopoulou, S.; Normand, P. Recent Advances in Nanoparticle Memories. *Mater. Sci. Eng., B* **2005**, *124−125*, 93−101.

(17) Kim, H.; Woo, S.; Kim, H.; Bang, S.; Kim, Y.; Choi, D.; Jeon, H. Pt Nanocrystals Embedded in Remote Plasma Atomic-Layer-Deposited HfO_2 for Nonvolatile Memory Devices. *Electrochem. Solid-State Lett.* **2009**, *12*, H92−H94.

(18) Kim, Y.; Park, K. H.; Chung, T. H.; Bark, H. J.; Yi, J.-Y.; Choi, W. C.; Kim, E. K.; Lee, J. W.; Lee, J. Y. Ultralarge Capacitance-Voltage Hysteresis and Charge Retention Characteristics in Metal Oxide Semiconductor Structure Containing Nanocrystals Deposited by Ion-Beam-Assisted Electron Beam Deposition. *Appl. Phys. Lett.* **2001**, *78*, 934−936.

(19) Gupta, R. K.; Krishnamoorthy, S.; Kusuma, D. Y.; Lee, P. S.; Srinivasan, M. P. Enhancing Charge-Storage Capacity of Non-Volatile Memory Devices using Template-Directed Assembly of Gold Nanoparticles. *Nanoscale* **2012**, *4*, 2296−2300.

(20) Leong, W. L.; Lee, P. S.; Mhaisalkar, S. G.; Chen, T. P.; Dodabalapur, A. Charging Phenomena in Pentacene-Gold Nanoparticle Memory Device. *Appl. Phys. Lett.* **2007**, *90*, 042906-3.

(21) Puniredd, S. R.; Yin, C. M.; Hooi, Y. S.; Lee, P. S.; Srinivasan, M. P. Dendrimer-Encapsulated Pt Nanoparticles in Supercritical Medium: Synthesis, Characterization, and Application to Device Fabrication. *J. Colloid Interface Sci.* **2009**, *332*, 505−510.

(22) Zhang, F.; Srinivasan, M. P. Multilayered Gold-Nanoparticle/Polyimide Composite Thin Film through Layer-by-Layer Assembly. *Langmuir* **2007**, *23*, 10102−10108.

(23) Krishnamoorthy, S.; Pugin, R.; Brugger, J.; Heinzelmann, H.; Hinderling, C. Tuning the Dimensions and Periodicities of Nanostructures Starting from the Same Polystyrene-block-Poly(2-vinylpyridine) Diblock Copolymer. *Adv. Funct. Mater.* **2006**, *16*, 1469−1475.

(24) Suresh, V.; Madapusi, S.; Krishnamoorthy, S. Hierarchically Built Hetero-superstructure Arrays with Structurally Controlled Material Compositions. *ACS Nano* **2013**, *7*, 7513−7523.

(25) Shin, D. O.; Mun, J. H.; Hwang, G.-T.; Yoon, J. M.; Kim, J. Y.; Yun, J. M.; Yang, Y.-B.; Oh, Y.; Lee, J. Y.; Shin, J.; Lee, K. J.; Park, S.; Kim, J. U.; Kim, S. O. Multicomponent Nanopatterns by Directed Block Copolymer Self-Assembly. *ACS Nano* **2013**, *7*, 8899−8907.

(26) Aizawa, M.; Buriak, J. M. Block Copolymer-Templated Chemistry on Si, Ge, InP, and GaAs Surfaces. *J. Am. Chem. Soc.* **2005**, *127*, 8932−8933.

(27) Yun, S.-H.; Yoo, S. I.; Jung, J. C.; Zin, W.-C.; Sohn, B.-H. Highly Ordered Arrays of Nanoparticles in Large Areas from Diblock Copolymer Micelles in Hexagonal Self-Assembly. *Chem. Mater.* **2006**, *18*, 5646−5648.

(28) Bennett, R. D.; Xiong, G. Y.; Ren, Z. F.; Cohen, R. E. Using Block Copolymer Micellar Thin Films as Templates for the Production of Catalysts for Carbon Nanotube Growth. *Chem. Mater.* **2004**, *16*, 5589−5595.

(29) Spatz, J. P.; Sheiko, S.; Möller, M. Ion-Stabilized Block Copolymer Micelles: Film Formation and Intermicellar Interaction. *Macromolecules* **1996**, *29*, 3220−3226.

(30) Hyejung, C.; Byung-Sang, C.; Tae-Wook, K.; Seung-Jae, J.; Man, C.; Takhee, L.; Hyunsang, H. Memory Characteristics of a Self-Assembled Monolayer of Pt Nanoparticles as a Charge Trapping Layer. *Nanotechnology* **2008**, *19*, 305704.

(31) Krishnamoorthy, S.; Manipaddy, K. K.; Yap, F. L. Wafer-Level Self-Organized Copolymer Templates for Nanolithography with sub-50 nm Feature and Spatial Resolutions. *Adv. Funct. Mater.* **2011**, *21*, 1102−1112.

(32) Suresh, V.; Huang, M. S.; Srinivasan, M. P.; Guan, C.; Fan, H. J.; Krishnamoorthy, S. Robust, High-Density Zinc Oxide Nanoarrays by Nanoimprint Lithography-Assisted Area-Selective Atomic Layer Deposition. *J. Phys. Chem. C* **2012**, *116*, 23729−23734.

(33) Suresh, V.; Huang, M. S.; Srinivasan, M. P.; Krishnamoorthy, S. Macroscopic High Density Nanodisc Arrays of Zinc Oxide Fabricated by Block Copolymer Self-Assembly Assisted Nanoimprint Lithography. *J. Mater. Chem.* **2012**, *22*, 21871−21877.

(34) Suresh, V.; Huang, M. S.; Srinivasan, M. P.; Krishnamoorthy, S. In Situ Synthesis of High Density sub-50 nm ZnO Nanopatterned Arrays Using Diblock Copolymer Templates. *ACS Appl. Mater. Interfaces* **2013**, *5*, 5727−5732.

(35) Park, S.; Lee, D. H.; Xu, J.; Kim, B.; Hong, S. W.; Jeong, U.; Xu, T.; Russell, T. P. Macroscopic 10-Terabit-per-Square-Inch Arrays from Block Copolymers with Lateral Order. *Science* **2009**, *323*, 1030−1033.

(36) Park, M.; Harrison, C.; Chaikin, P. M.; Register, R. A.; Adamson, D. H. Block Copolymer Lithography: Periodic Arrays of ~1011 Holes in 1 Square Centimeter. *Science* **1997**, *276*, 1401−1404.

(37) Grabar, K. C.; Freeman, R. G.; Hommer, M. B.; Natan, M. J. Preparation and Characterization of Au Colloid Monolayers. *Anal. Chem.* **1995**, *67*, 735−743.

DOI: 10.1021/am506174s
ACS Appl. Mater. Interfaces 2015, 7, 279−286

(38) Yap, F. L.; Thoniyot, P.; Krishnan, S.; Krishnamoorthy, S. Nanoparticle Cluster Arrays for High-Performance SERS through Directed Self-Assembly on Flat Substrates and on Optical Fibers. *ACS Nano* **2012**, *6*, 2056−2070.
(39) Chan, M. Y.; Lee, P. S.; Ho, V.; Seng, H. L. Ge Nanocrystals in Lanthanide-Based Lu_2O_3 High-k Dielectric for Nonvolatile Memory Applications. *J. Appl. Phys.* **2007**, *102*, 094307-7.
(40) Nicollian, E. H.; Brews, J. R. *MOS /Metal Oxide Semiconductor/ Physics and Technology*; Wiley: New York, 1982; p 920.
(41) Tiwari, S.; Rana, F.; Chan, K.; Shi, L.; Hanafi, H. Single Charge and Confinement Effects in Nanocrystal Memories. *Appl. Phys. Lett.* **1996**, *69*, 1232−1234.
(42) Kim, J. K.; Cheong, H. J.; Kim, Y.; Yi, J.-Y.; Bark, H. J.; Bang, S. H.; Cho, J. H. Rapid-Thermal-Annealing Effect on Lateral Charge Loss in Metal-Oxide-Semiconductor Capacitors with Ge Nanocrystals. *Appl. Phys. Lett.* **2003**, *82*, 2527−2529.
(43) Liu, Z.; Lee, C.; Narayanan, V.; Pei, G.; Kan, E. C. Metal Nanocrystal Memories-Part II: Electrical Characteristics. *IEEE Trans. Electron Devices* **2002**, *49*, 1614−1622.

DOI: 10.1021/am506174s
ACS Appl. Mater. Interfaces 2015, 7, 279−286